SUMMARY OF THE INVENTION

The present invention provides for a method for testing a circuit under realistic conditions. Furthermore, embodiments provide for such a method that does not require time consuming programming. Furthermore, embodiments provide for such a method that is cost effective. Additionally, embodiments provide for such a method that allows easy switching between test mode and normal mode. The present invention provides these advantages and others not specifically mentioned above but described in the sections to follow.

A method for applying instructions to a microprocessor during test mode is disclosed. In one embodiment of the present invention, first a test mode is entered, establishing the microprocessor as a slave and a test controller as a master. Then, the test controller fills an instruction queue with instructions to be executed. The instructions originate from a test interface. A memory, such as a program flash, coupled to the microprocessor is bypassed; thus, the microprocessor is forced to execute instructions from the instruction queue.

Another embodiment provides for an architecture for applying instructions to a microprocessor during test mode. The architecture comprises a microprocessor coupled to a bus, an instruction queue coupled to the microprocessor and to the bus, a test controller coupled to the bus, and a supervisory memory coupled to the microprocessor. The supervisory memory comprises pre-determined test instructions. The test controller is operable to load instructions received from a test interface into the instruction queue.

Still another embodiment provides for a method in which first a test mode is entered, establishing the microprocessor as a slave and a test controller as a master. Next, the test controller transfers to a queue an instruction to be executed in the microprocessor. Then, the instruction causes instructions from a supervisory memory to be executed by the microprocessor. The supervisory memory comprises pre-determined test instructions.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a diagram of a system for testing a circuit, according to embodiments of the present invention.

Figure 2 is a diagram of an architecture for providing an interface to test a circuit, according to embodiments of the present invention.

Figure 3 is a diagram of an architecture for providing an interface to test a circuit, according to embodiments of the present invention.

Figure 4 is a flowchart of steps of a process of applying instructions to a microprocessor during test mode, according to an embodiment of the present invention.

Figure 5 is a flowchart of steps of a process of applying instructions to a microprocessor during test mode and switching between on-chip and off-chip instructions, according to an embodiment of the present invention.

Figure 6 is a diagram of traces indicating the sequence of events that occur during entering chip test mode, according to embodiments of the present invention.

Figure 7 is a flowchart illustrating the steps of a process of entering circuit test mode, according to an embodiment of the present invention.